Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Original): A method of testing a probe card comprising the steps of:

positioning the probe card in a prober over a verification wafer;

bringing the probe card in contact with a contact region on the verification wafer, the verification wafer including a shorting plane surrounding the contact region;

sending a test signal through the contact region to the probe card; and

receiving a response signal from the probe card through the verification wafer.

Claim 2 (Original): The method of claim 1, further including the step of receiving the response signal over a cable attached to the verification wafer.

Claim 3 (Original): The method of claim 1, further including the step of continuously sending test signals through the verification wafer while bringing the verification wafer in contact with the probe card so as to measure height of probes on the probe card.

Claim 4 (Currently amended): The method of claim 1, further including the step of performing a continuity test on a signal path ~~between a test signal generator and~~ in the probe card.

Claim 5 (Original): The method of claim 4, further including the step of using time domain reflectometry (TDR) to perform the continuity test.

Claim 6 (Original): The method of claim 4, further including the step of using frequency domain reflectometry (FDR) to perform the continuity test.

Claim 7 (Currently amended): The method of claim 1, further including the step of determining impedance of a signal path ~~between a test signal generator that sends the test signal and~~ in the probe card.

Claim 8 (Original): The method of claim 1, further including the step of testing leakage current in the probe card.

Claim 9 (Original): The method of claim 1, further including the step of measuring planarity of the probe card by bringing the probe card and the verification wafer together until probes of the probe card make contact with the verification wafer, and measuring a position of the verification wafer along a direction perpendicular to the verification wafer.

Claim 10 (Original): The method of claim 1, further including the step of verifying location of probes of the probe card.

Claim 11 (Original): The method of claim 1, further including the steps of:

bringing the probe card in contact with a plurality of contact regions on the verification wafer during the step of bringing the probe card in contact with the contact region;

sending test signals through the contact regions on the verification wafer to the probe card; and

receiving response signals from the probe card.

Claim 12 (Original): A method of testing a probe card comprising the steps of:

positioning the probe card having probes in a prober over a blank wafer;

bringing the probe card in contact with the blank wafer;

making scrub marks on the blank wafer with the probes by moving the blank wafer in an X, Y plane; and

examining the scrub marks on the blank wafer to determine location of the probes.

Claim 13 (Original): A method of testing a probe card comprising the steps of:

placing a verification wafer in a prober, the verification wafer having a contact region, a shorting plane surrounding the contact region, and an electrical connection to a tester;

positioning the probe card in the prober over the verification wafer;

bringing the probe card in contact with the contact region;

generating a test signal in the tester;

transmitting the test signal to the probe card through the contact region; and

receiving a response signal from the probe card over the electrical connection.

Claim 14 (Original): The method of claim 13, wherein the electrical connection includes a cable attached to the verification wafer.

Claim 15 (Original): The method of claim 13, further including the step of continuously sending test signals through the verification wafer while bringing the verification wafer in contact with the probe card so as to measure height of probes on the probe card.

Claim 16 (Original): The method of claim 13, further including the step of performing a continuity test on a signal path between a test signal generator and the probe card.

Claim 17 (Original): The method of claim 16, further including the step of using time domain reflectometry (TDR) to perform the continuity test.

Claim 18 (Original): The method of claim 16, further including the step of using frequency domain reflectometry (FDR) to perform the continuity test.

Claim 19 (Original): The method of claim 13, further including the step of determining impedance of a signal path between a test signal generator and the probe card.

Claim 20 (Original): The method of claim 13, further including the step of testing leakage current in the probe card.

Claim 21 (Original): The method of claim 13, further including the step of measuring planarity of the probe card by bringing the probe card and the verification wafer together until probes of the probe card make contact with the verification wafer, and measuring a position of the verification wafer along a direction perpendicular to the verification wafer.

Claim 22 (Original): The method of claim 13, further including the step of verifying location of probes of the probe card.

Claim 23 (Original): The method of claim 13, further including the steps of:

bringing the probe card in contact with a plurality of contact regions on the verification wafer during the step of bringing the probe card in contact with the contact region;

sending test signals through the contact regions to the probe card; and

receiving response signals from the probe card.

Claim 24 (Original): A system for testing a probe card comprising:

a prober including means for moving a verification wafer in at least a vertical direction;

a verification wafer positioned on means for moving and having a contact region surrounded by a shorting plane;

an electrical connection from the contact region to a test signal generator,

wherein signals generated by the test signal generator are transmitted to a probe on a probe card under test.

Claim 25 (Original): The system of claim 24, wherein the verification wafer includes a plurality of contact regions surrounded by the shorting plane for testing multiple probes on the probe card under test.

Claim 26 (Original): The system of claim 24, wherein the electrical connection is one of a coaxial cable and a flex cable.

Claim 27 (Original): The system of claim 24, wherein the test generator includes a time domain reflectometry apparatus.

Claim 28 (Original): The system of claim 24, wherein the test generator includes a frequency domain reflectometry apparatus.